

**REMARKS/ARGUMENTS**

The claims are modified in the amendment. More specifically, claims 9, 13, 18, 20, and 23 are cancelled; and dependent claims 31-35 have been added; no claims have been amended. Therefore, claims 1-8, 10-12, 14-17, 19, 21, 22, 24-35 are present for examination. No new matter is added by these amendments. Applicant respectfully requests reconsideration of this application as amended.

**35 U.S.C. §102/103 Rejections**

The Final Office Action dated May 20, 2005 rejected claims 1-5, 7, 9-15, 18, 29, and 30 under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,338,160 to Patel et al. (hereinafter "Patel"). That Office Action rejected claims 19, 20, 24, 26 and 28 under 35 U.S.C. §102(e) as being anticipated by the cited portions of U.S. Patent No. 6,366,999 to Drabenstott et al. (hereinafter "Drabenstott"). Next, the Office Action rejected claims 6 and 16 under 35 U.S.C. §103(a) as being unpatentable over Patel. The Office Action then rejected claims 21 and 23 under 35 U.S.C. §103(a) as being unpatentable over Drabenstott in view of Patel. Lastly, the Office Action has rejected claim 25 under 35 U.S.C. §103(a) as being unpatentable over Drabenstott. Applicants again assert that the PC register of the Patel reference is outside of the processing core.

In the amendment dated July 21, 2004, Applicants point out that:

Patel is cited for the proposition that a register in the register file of the processing core holds the program counter value as required all claims. Reliance on Patel for this proposition goes too far. Patel has hardware JAVA registers **44** that are *outside* of CPU **25**. Patel, FIG. 3. Those JAVA registers hold the program counter (PC), but those JAVA registers are *not* within the processing core "and should not be confused with the general registers **46** or **48** which are operated upon by the central processing unit **26**."...Considering the whole of Patel, it is clear that the PC is not in the register file of the processing core.

However, in the Final Office Action dated May 20, 2005, the Office stated that "the whole system 20 comprising JAVA accelerator (detailed structure shown in Fig. 3) is best reasonably *and broadly* interpreted as a processing unit or core" (*Emphasis added*, Final Office Action, page 14, ¶ 10). Applicants respectfully assert that this interpretation is too broad.

Patel has hardware JAVA registers 44 which hold the program counter ("PC") that are *outside* of the CPU 25. The PC of the present invention is included in the processing pipeline of the processing core. While there may be no universal definition of "processing core," those of ordinary skill in the art recognize that a "processing core" is necessarily within a CPU. In broad interpretations, processing core may be used synonymously with CPU. However, applicants assert that a "processing core" is not outside of the CPU as those terms are reasonably understood by those of skill in the art.

In light of the foregoing, claims 1-8, 10-12, 14-17, 19, 21, 22, and 24-35 are in condition for allowance.

#### ***New Dependent Claims 31-35***

Claims 31-35 have been added to specify that the one or more register files (and thus the PC register as well) be *included within the processing pipeline* of the processing core, to address concerns which arose because of broad interpretation by the Office of the term "processing core." The new claims depend from the independent claims 1, 10, 19, 29 and 30, respectively. These new claims specify that the one or more register files be *included within the processing pipeline* of the processing core. One of these register files comprises a program counter ("PC") register. Support for the amendment is provided in the Application, filed March 8, 2001, (*see, e.g.*, Application, page 7, line 17 - page 8, line 4; Figs. 2 and 3). It is respectfully believed that neither Patel or Drabentstott teach or suggest that a PC register be included within the processing pipeline.

I. Patel: In Patel, the "CPU 26 is divided into pipeline stages including the instruction fetch 26a, instruction decode 26b, execute logic 26c, memory access logic 26d, and writeback logic 26e" (Patel Patent, col. 5, lines 43-45). In Patel, the hardware Java registers 44 which hold the PC register are **not included within this processing pipeline**. It is further evident

from Fig. 3 of Patel that the PC (located in the hardware Java registers) is not located within the processing pipeline (*Id.*, Fig. 3).

In light of the foregoing, dependent claims 31, 32, 34, and 35 are allowable for at least the reasons given above.

II. Drabenstott: The Office rejected the independent claim 19 as being anticipated by Drabenstott, and new dependent claim 33 depends from claim 19. However, in Final Office Action dated May 20, 2005, the office cites *Patel* for the proposition that "one of (the registers) comprises a program counter register" when addressing claim 19 (Final office Action, page 7, lines 11-14). As illustrated above, the claims fall outside of the scope of Patel. Further, there is no indication in Drabenstott where the PC register is located.

In light of the foregoing, independent claim 33 is allowable for at least the reasons given above.

### **Drawing Objection**

Jump tables hold address values for the jump destinations or can merely hold an offset value from the program counter. "Jump tables" are comprised of jump instructions which "typically are individual instructions within an instruction set" (Application, page 1, lines 28-29). Applicant notes that there is ample showing of "instructions." No change to the drawings is believed necessary to comply with 37 CFR 1.83(a) given ample showing in the current drawings.

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PATENT

**CONCLUSION**

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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